JEDEC STANDARD

Definition of the SSTU32S869 and SSTU32D869 Registered Buffer with Parity for DDR2 RDIMM Applications

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DEFINITION OF THE SSTU32S869 AND SSTU32D869 REGISTERED BUFFER FOR DDR2 WITH PARITY RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-97 and JCB-07-05, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32S869 and SSTU32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM.

The purpose is to provide a standard for the SSTU32S869 and SSTU32D869 (see Note) logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designations SSTU32S869 and SSTU32D869 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 14-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers optimized to drive the DDR2 DIMM load, following the SSTL_18 standard. They provide 50% more dynamic driver strength than the standard SSTU32864 outputs.

The SSTU32S869 and SSTU32D869 operate from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{\text{RESET}}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs except $\overline{\text{PTYERR}}$ are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. SSTU32S869 and SSTU32D869 must ensure that the outputs remain low as long as the data inputs are low, the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ and the input receivers are fully enabled. This will ensures that there are no glitches on the output.

2 Device Standard (cont'd)

2.1 Description (cont'd)

If the data inputs are not held low, then $\overline{DCS}$ and $\overline{CSR}$ must be held high, DODT and DCKE must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{RESET}$.

The parity error output $\overline{PTYERR}$ will be reset to high by $\overline{RESET}$ transitioning low and will not be decoded until after $\overline{RESET}$ goes high and $\overline{DCS}$ and/or $\overline{CSR}$ are asserted low.

The device monitors both $\overline{DCS}$ and $\overline{CSR}$ inputs and will gate the Qn, PPO (Partial-Parity-Out) and $\overline{PTYERR}$ (Parity Error) Parity outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ are high. If either $\overline{DCS}$ or $\overline{CSR}$ input is low, the Qn, PPO and $\overline{PTYERR}$ outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ controls and will force the Qn and PPO outputs low and the $\overline{PTYERR}$ high.

The SSTU32S869 and SSTU32D869 include a parity checking function. The SSTU32S869 and SSTU32D869 accept a parity bit from the memory controller at its input pin PARIN one or two cycles after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain $\overline{PTYERR}$ pin (active low) whether a parity error has occurred. The number of cycles depends on the setting of C1/C2, see Figure 6 and 7.

When used as a single device, the C1/C2 inputs are tied low. When used in pairs, the C1/C2 inputs are tied low for the first register (front) and the C1/C2 inputs are tied high for the second register. When used as a single register, the PPO and $\overline{PTYERR}$ signals are produced two clock cycles after the corresponding data input. When used in pairs, the $\overline{PTYERR}$ signals of the first register are left floating. The PPO outputs of the first register are cascaded to the PARIN signals on the second register (back). The PPO and $\overline{PTYERR}$ signals of the second register are produced three clock cycles after the corresponding data input. Parity implementation and device wiring for single and dual die is described in Figure 1.

If an error occurs, and the $\overline{PTYERR}$ is driven low, it stays low for two clock cycles or until $\overline{RESET}$ is driven low. The DIMM-dependent signals (DCKE, $\overline{DCS}$, $\overline{CSR}$ and DODT) are not included in the parity check computations.

All registers used on an individual DIMM must be of the same configuration, i.e., single or dual die.

2 Device Standard (cont'd)

2.1 Description (cont'd)

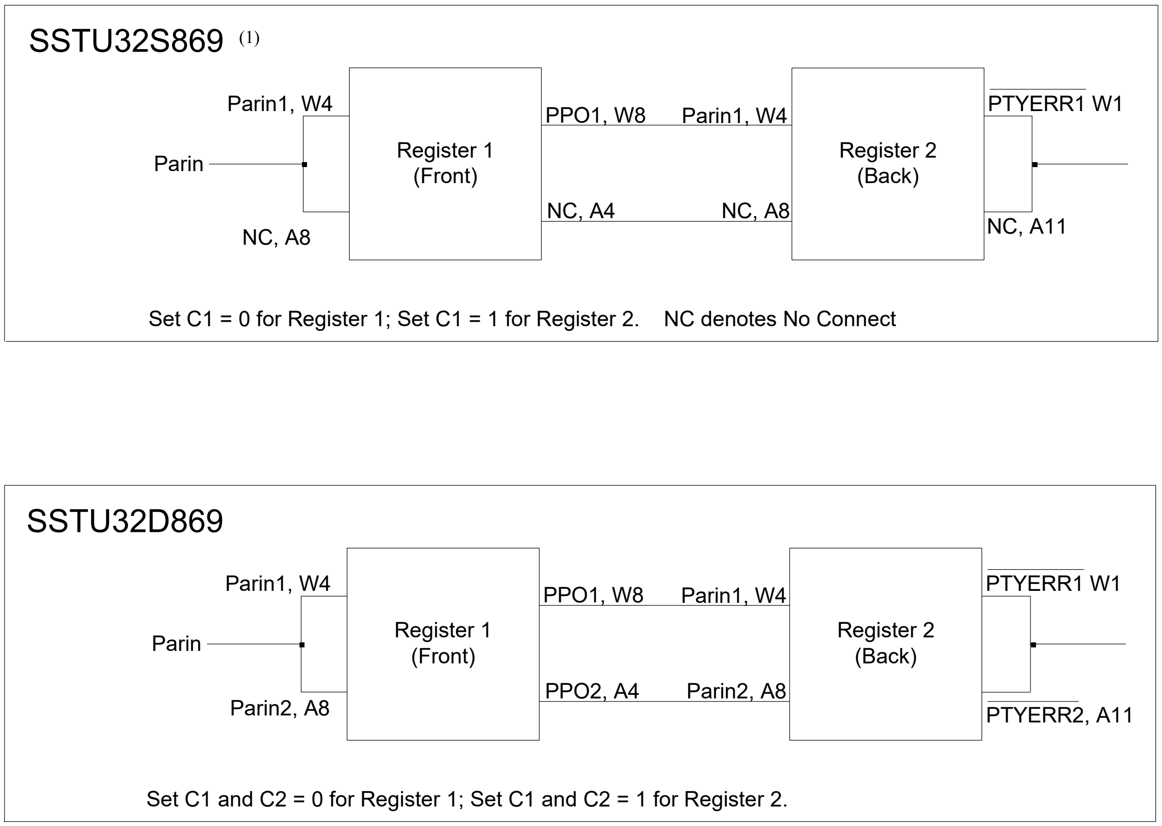


Figure 1 — Parity Implementation and Device Wiring for SSTU32S869 and SSTU32D869

2 Device Standard (cont'd)

Package options include 150-ball Thin Profile Fine Pitch BGA (TFBGA) (11 × 19 array, 8.0 × 13.0 mm body size, 0.65 mm pitch, MO-225, Variation TBD).

2.2 150-ball TFBGA (MO-225xx)

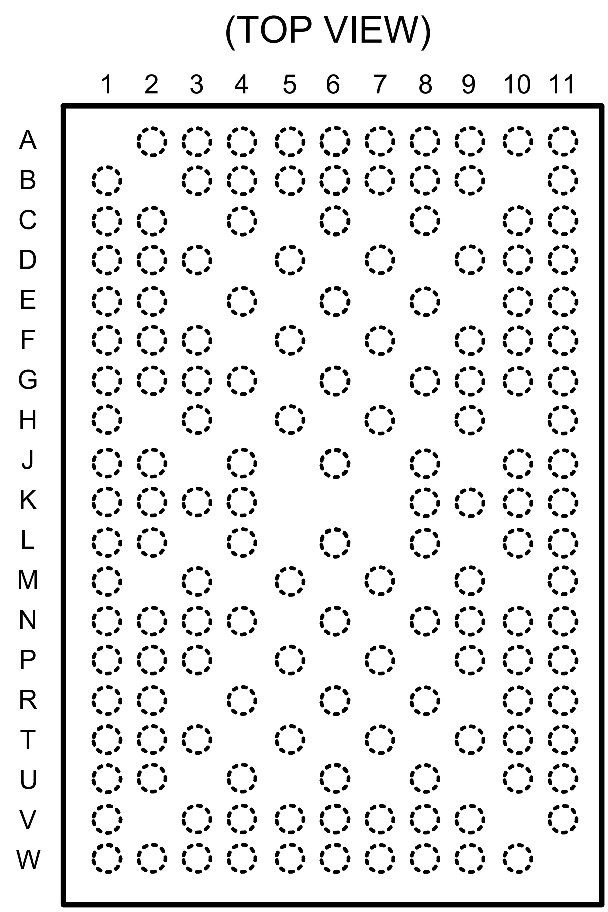


Figure 2 — Pinout Configuration

2 Device Standard (cont'd)

2.3 Pinout Top View for 150-ball TFBGA

150-ball, 11 × 19 grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	NB	VDD	MCL(1)	PP02(2)	GND	VREF	GND	PARIN2(2)	MCL(1)	VDD	$\overline{\text{PTYERR2}}$(2)
B	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
C	QCKEA	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	QCKEB
D	Q2A	VDD	GND	NB	DCKE	NB	D2	NB	GND	VDD	Q2B
E	Q3A	VDD	NB	D3	NB	NC	NB	DODT	NB	C2(2)	Q3B
F	QODTA	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	QODTB
G	Q5A	VDD	GND	D5	NB	CLK	NB	D6	GND	VDD	Q5B
H	Q6A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q6B
J	$\overline{\text{QCSA}}$	VDD	NB	NC	NB	$\overline{\text{RESET}}$	NB	$\overline{\text{CSR}}$	NB	VDD	$\overline{\text{QCSB}}$
K	VDD	VDD	GND	GND	NB	NB	NB	GND	VDD	VDD	VDD
L	Q8A	VDD	NB	$\overline{\text{DCS}}$	NB	$\overline{\text{CLK}}$	NB	D8	NB	VDD	Q8B
M	Q9A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q9B
N	Q10A	VDD	GND	D9	NB	NC	NB	D10	GND	VDD	Q10B
P	Q11A	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	Q11B
R	Q12A	C1	NB	D11	NB	NC	NB	D12	NB	VDD	Q12B
T	Q13A	VDD	GND	NB	D13	NB	D14	NB	GND	VDD	Q13B
U	Q14A	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	Q14B
V	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
W	$\overline{\text{PTYERR1}}$	VDD	MCL(1)	PARIN1	GND	VREF	GND	PPO1	MCL(1)	VDD	NB

NB indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die).

Figure 3 — Pinout Top View for 150-ball TFBGA

NOTE 1 MCL denotes input pin that must be connected Low. Register Vendors: Implement NC or input on Ball A3, A9, W3, W9

NOTE 2 NC for single die version

2 Device Standard (cont'd)

2.4 Terminal Functions

Table 1 — Terminal Functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE, DODT	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D1 ... D14 [1]	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{DCS}$, $\overline{CSR}$	SSTL_18	DRAM Chip Select signals. This pins initiate DRAM address/ command decodes, and as such at least one will be low when a valid address/command is present.
Re-driven outputs	Q1A...Q14A, Q1B ... Q14B, $\overline{QCSA}$,$\overline{QCSB}$ QCKEA,QCKEB QODTA,QODTB	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN1, PARIN2 [2]	SSTL_18	Input parity is received on pin PARIN and should maintain parity across the D1...D14(1) inputs, at the rising edge of the clock, one clock cycle after Chip Select is LOW.
Parity output	PPO1, PPO2 [2]	SSTL_18	Partial Parity Output. Indicates parity out of D1-D14 [1]
Parity error output	$\overline{PTYERR1}$, $\overline{PTYERR2}$ [2]	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by in total 2 clock cycles for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition).
Configuration Inputs	$\overline{C1, C2}$	1.8V LVCMOS	When Low, register is configured as Register 1. When High, register is configured as Register 2.
Clock inputs	CK, $\overline{CK}$	SSTL_18	Differential main clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	$\overline{RESET}$	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.
	VDD	Power Input	Power supply voltage
	GND	Ground Input	Ground

NOTE 1 Inputs D1, D4, D7, and their corresponding outputs Qn are not included in this range.
NOTE 2 NC for single die version.

2 Device Standard (cont'd)

2.5 Function Table

Table 2 — Function Table (each Flip Flop)

Inputs						Outputs		
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODT, DCKE	Qn	$\overline{QCS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	↑	↓	L	Q_0	H	L
H	H	H	↑	↓	H	Q_0	H	H
H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

2 Device Standard (cont'd)

2.5 Function Table (cont'd)

Table 3 — Parity and Standby Function Table

Inputs							Output	
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Σ of inputs = H D1...D14 [1]	PARIN1 [2], PARIN2 [4]	PPO1 [2], PPO2 [4]	$\overline{\text{PTYERR1}}$ [3] $\overline{\text{PTYERR2}}$
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	L	L	↑	↓	Even	L	L	H
H	L	L	↑	↓	Odd	L	H	L
H	L	L	↑	↓	Even	H	H	L
H	L	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	$PPOn_0$	$\overline{PTYERRn}_0$
H	X	X	L or H	L or H	X	X	$PPOn_0$	$\overline{PTYERRn}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	H

NOTE 1 Inputs D1, D4, and D7 are not included in this range.

NOTE 2 PARIN1 and PARIN2 arrives one (C1, C2 =0) or two (C1, C2=1) clock cycles after data to which it applies.

NOTE 3 This transition assumes $\overline{\text{PTYERR}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{PYTERR}}$ is low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. PARIN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. PARIN2 is used to generate PPO2 and $\overline{\text{PTYERR2}}$.

NOTE 4 PARIN2, PPO2 and $\overline{\text{PTYERR2}}$ not required for single die.

2 Device Standard (cont'd)

2.6 Logic Diagram

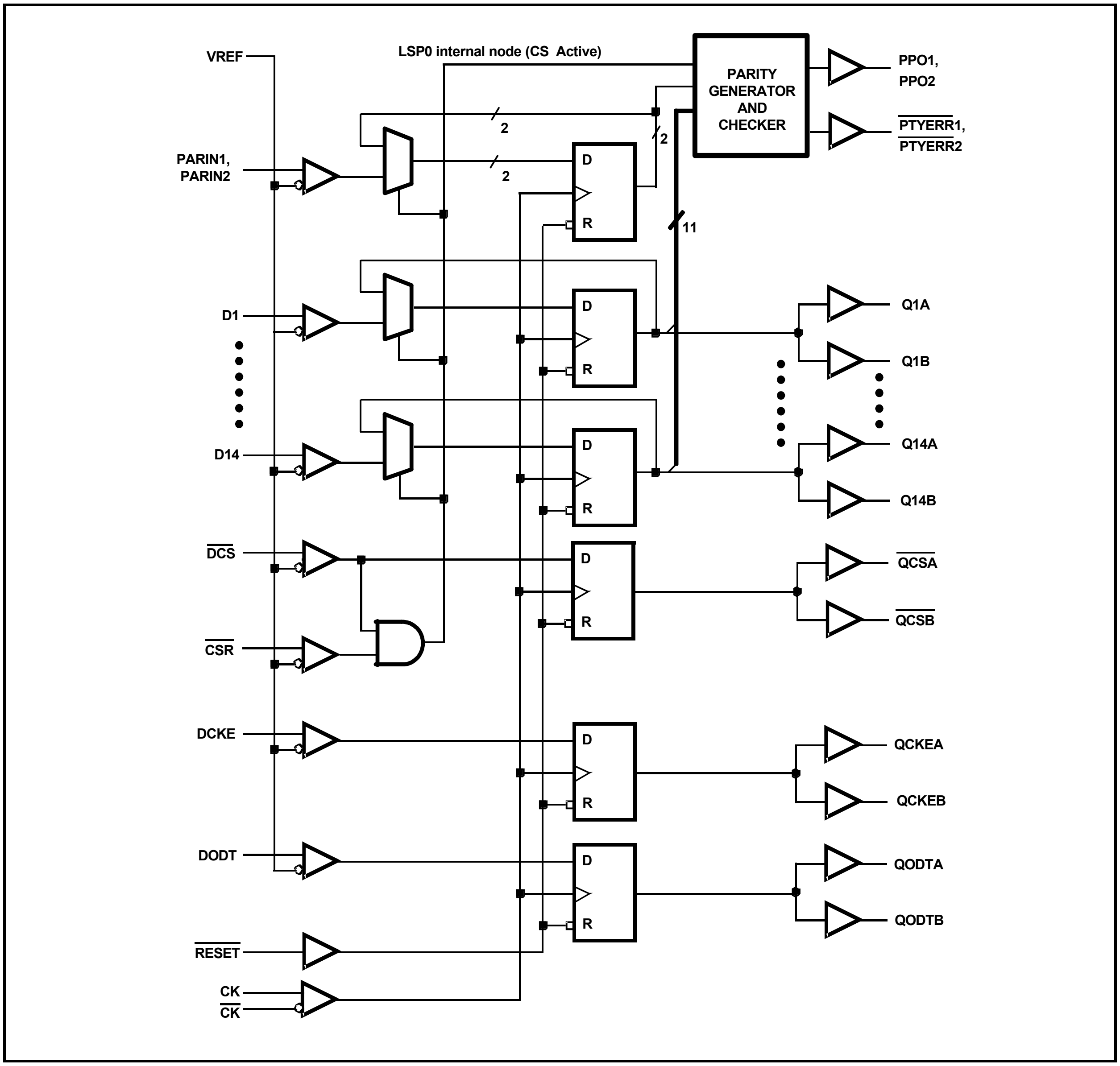
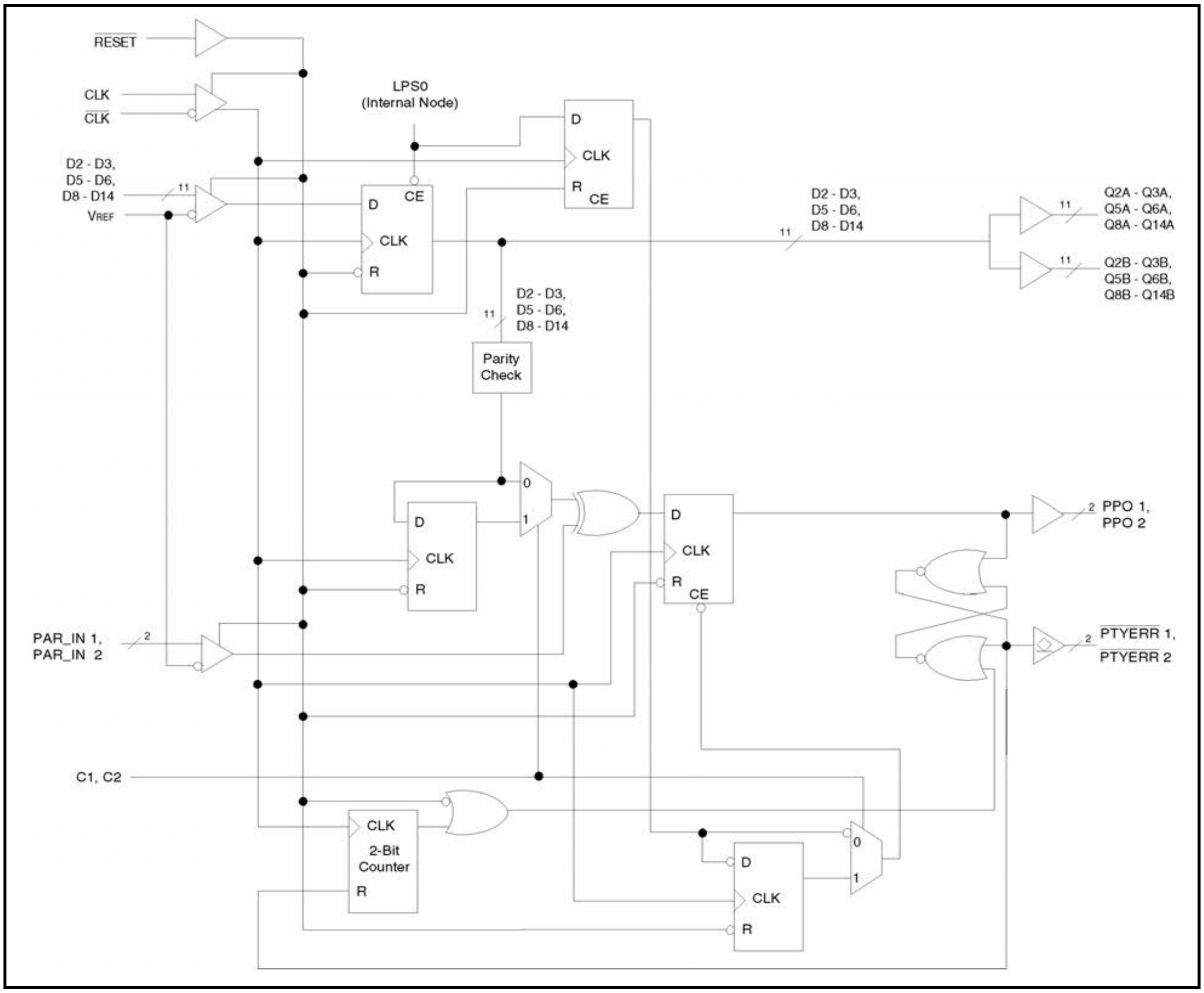


Figure 4 — Logic Diagram (Positive Logic)

2 Device Standard (cont'd)

2.7 Register Timing



NOTE 1 PARIN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. PARIN2 is used in the dual die version to generate PPO2 and $\overline{\text{PTYERR2}}$. PARIN2, PPO2 and $\overline{\text{PTYERR2}}$ are not present in single die versions.

Figure 5 — Timing of Clock, Data, and Parity Signals

2 Device Standard (cont'd)

2.7 Register Timing (cont'd)

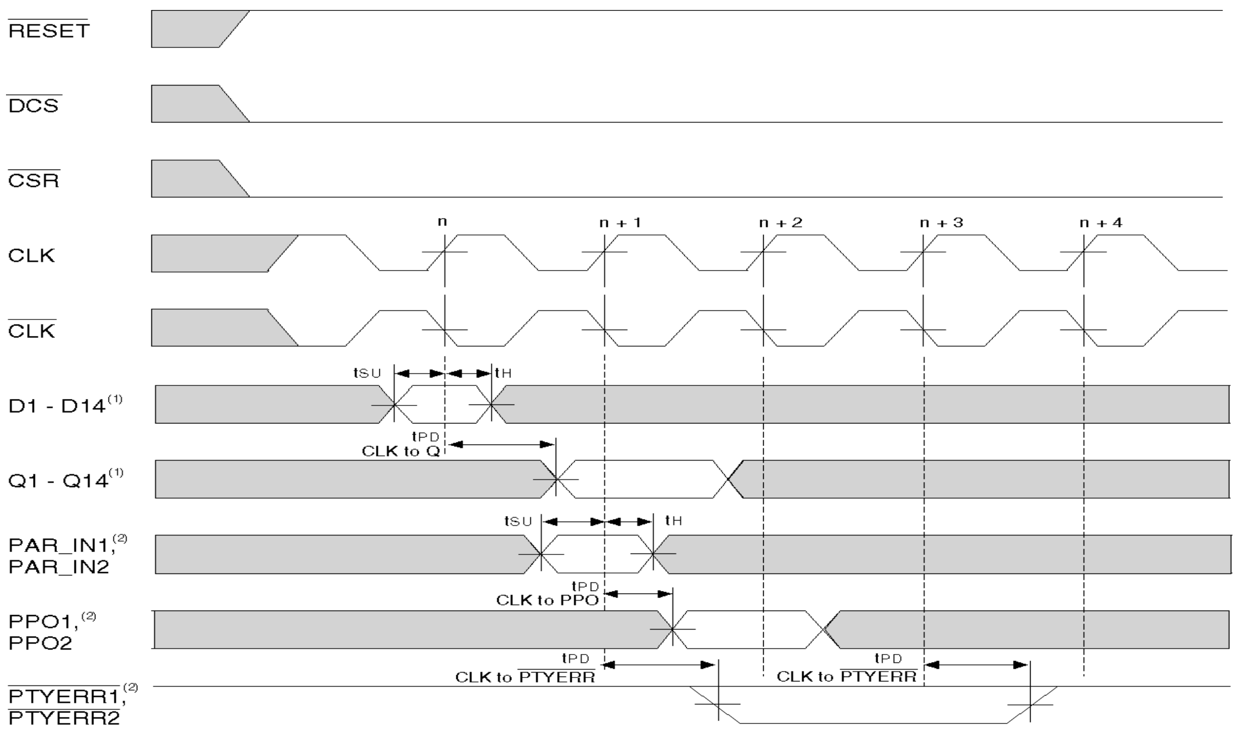


Figure 6 — Timing Diagram for the 1st SSTU32S869 and SSTU32D869 C1/C2=0

NOTE 1 This range does not include D1, D4, D7, and their corresponding outputs

NOTE 2 PARIN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. In SSTU32D869 PARIN2 is used to generate PPO2 and $\overline{\text{PTYERR2}}$

2 Device Standard (cont'd)

2.7 Register Timing (cont'd)

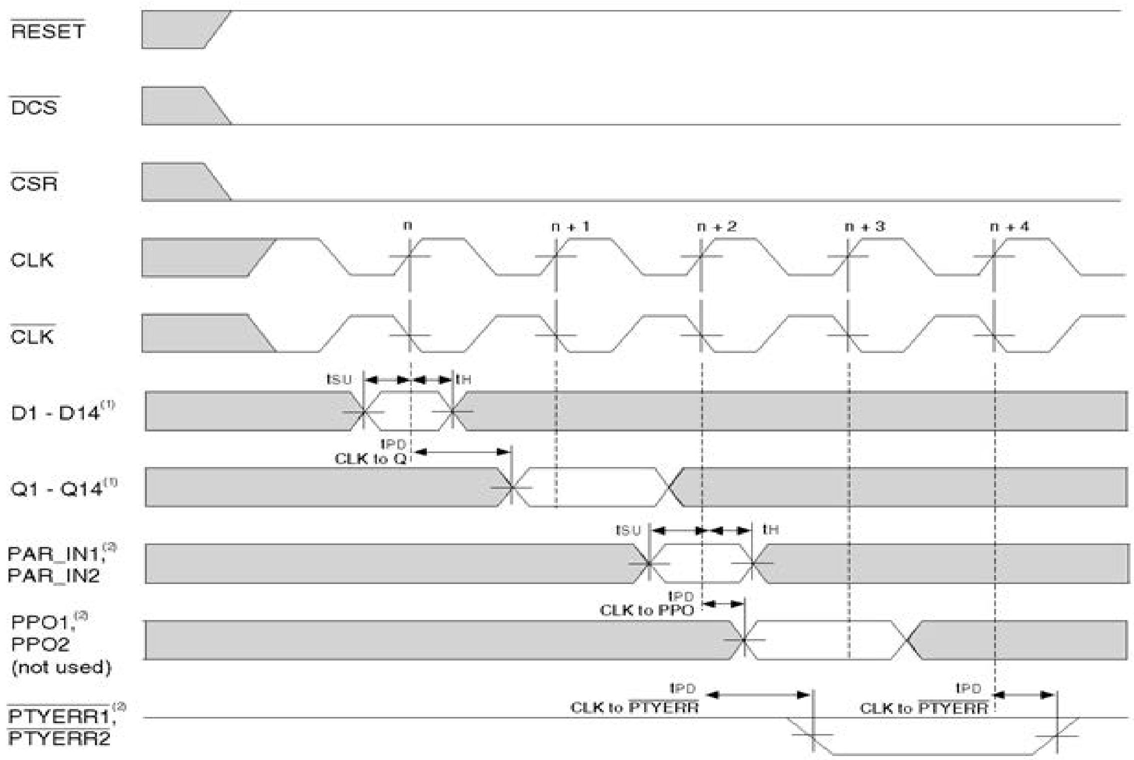


Figure 7 — Timing Diagram for the 2nd SSTU32S869 and SSTU32D869, C1/C2=1

NOTE 1 This range does not include D1, D4, D7, and their corresponding outputs

NOTE 2 PARIN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. In SSTU32D869 PARIN2 is used to generate PPO2 and $\overline{\text{PTYERR2}}$

2 Device standard (cont'd)

2.7 Register Timing (cont'd)

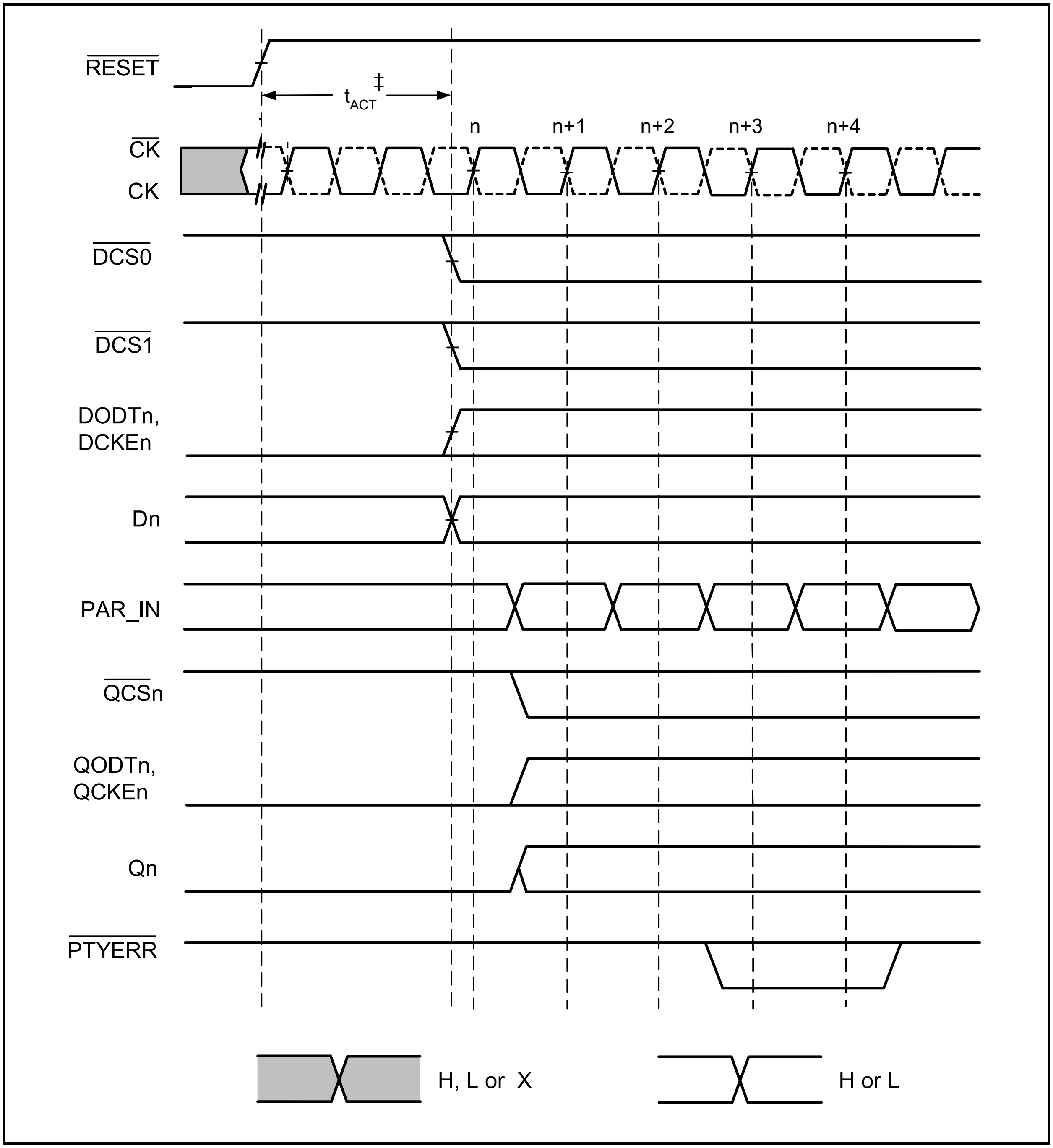


Figure 8 — Timing Diagram during Start-up when Data Inputs are Low or High (RESET Switches from L to H)

‡ After RESET is switched from low to high, DCS and CSR must be held HIGH, DODT and DCKE must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

2 Device Standard (cont'd)

2.8 Absolute Maximum Ratings

Table 4 — Absolute Maximum Ratings over Operating Free-air Temperature Range [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	+2.5	V
V_I	Receiver input voltage	See NOTES 2 and 3	–0.5	+2.5	V
V_O	Driver output voltage	See NOTES 2 and 3	–0.5	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	Storage temperature		–65	+150	°C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 3.6 V maximum.

Table 5 — Mode Select

C1/C2	Device Mode
0	First Device in Pair, Front
1	Second Device in Pair, Back

2 Device Standard (cont'd)

2.9 Recommended Operating Conditions

Table 6 — Recommended Operating Conditions (see NOTE 1)

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	Supply voltage		1.7	-	1.9	V
V_{REF}	Reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	Termination voltage		$V_{REF} – 40$ mV	V_{REF}	$V_{REF} + 40$ mV	V
V_I	Input voltage		0	-	V_{DD}	V
V_{IH}	AC HIGH-level input voltage	Data inputs	$V_{REF} + 250$ mV	-	-	V
V_{IL}	AC LOW-level input voltage	Data inputs	-	-	$V_{REF} – 250$ mV	V
V_{IH}	DC HIGH-level input voltage	Data inputs	$V_{REF} + 125$ mV	-	-	V
V_{IL}	DC LOW-level input voltage	Data inputs	-	-	$V_{REF} – 125$ mV	V
V_{IH}	HIGH-level input voltage	$\overline{\text{RESET}}$	$0.65 \times V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	$\overline{\text{RESET}}$	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	Common-mode input voltage range	CK, $\overline{\text{CK}}$	0.675	-	1.125	V
V_{ID}	Differential input voltage	CK, $\overline{\text{CK}}$	600	-	-	mV
I_{OH}	HIGH-level output current		-	-	-8	mA
I_{OL}	LOW-level output current		-	-	8	mA
I_{ERROL}	$\overline{\text{PTYERR}}$ LOW-level output current		25	-	-	mA
T_{amb}	Operating ambient temperature in free-air		0	-	+70	°C

NOTE 1 The $\overline{\text{RESET}}$ input of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is LOW.

2 Device Standard (cont'd)

2.10 DC Specifications

Table 7 — Electrical Characteristics over Recommended Operating Free-air Temperature Range

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = –6 mA		1.2	-	-	V
V_{ERROL}	$\overline{PTYERR}$ output LOW voltage	I_{ERROL} = 25 mA; V_{DD} = 1.7 V	-	-	0.5	V	
V_{OL}	Output LOW voltage	I_{OL} = 6 mA		-	-	0.5	V
I_I	Input current	All inputs, V_I = V_{DD} or GND		-	-	±5	µA
	Static standby current	$\overline{RESET}$ = GND		-	-	200	µA
I_{DD}							
	Static operating current	RESET = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$		-	-	80	mA
I_{DDD}	Dynamic operating current — clock only	$\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. I_O = 0; V_{DD} = 1.9 V		-	†	-	µA/ MHz
	Dynamic operating current — per each data input	$\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I_O = 0; V_{DD} = 1.9 V		-	†	-	µA/ MHz

NOTE † The vendor must supply this value for full device description.
NOTE † † The vendor must choose to comply with either single die or dual-die specification in accordance to the device implementation

Table 8 — Capacitance Values for Single Die Version (SSTU32S869)

C_i	Input capacitance, Data inputs	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, Parity input	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5		3.5	pF
	Input capacitance, $\overline{DCSn}$† † / $\overline{CSR}$	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5		3.5	
	Input capacitance, CK and $\overline{CK}$	V_{ICR} =0.9V; $V_{I(PP)}$ = 600mV; V_{DD} = 1.8 V	2		3	pF
	Input capacitance, $\overline{RESET}$	V_I = V_{DD} or GND; V_{DD} = 1.8 V	†	-	†	pF

Table 9 — Capacitance Values for Dual Die Version (SSTU32D869)

C_i	Input capacitance, Data inputs	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, Parity input	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, $\overline{DCSn}$† † / $\overline{CSR}$	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	4	-	6	pF
	Input capacitance, CK and $\overline{CK}$	V_{ICR} =0.9V; $V_{I(PP)}$ = 600mV; V_{DD} = 1.8 V	4	-	6	pF
	Input capacitance, $\overline{RESET}$	V_I = V_{DD} or GND; V_{DD} = 1.8 V	†	-	†	pF

2 Device Standard (cont'd)

2.11 Timing Requirements

Table 10 — Timing Requirements over Recommended Operating Free-air Temperature Range (see Figure 6)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clock}	Clock frequency		-	340	MHz
t_W	Pulse duration, CK, $\overline{CK}$ HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time	(see NOTES 1 and 2)	-	10	ns
t_{INACT}	Differential inputs inactive time	(see NOTES 1 and 3)	-	15	ns
t_{SU}	Setup time, Chip Select	Chip select valid before clock switching	0.5	-	ns
	Setup time, Data	D[n] valid before clock switching	0.3	-	ns
t_H	Hold time	Input to remain valid after clock switching	0.3	-	ns

NOTE 1 This parameter is not necessarily production tested.

NOTE 2 Data inputs must be active below a minimum time of t_{ACT} (max) after $\overline{RESET}$ is taken HIGH.

NOTE 3 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} (max) after $\overline{RESET}$ is taken LOW.

2 Device Standard (cont'd)

2.12 AC Specifications

Table 11 — Switching Characteristics over Recommended Operating Free-air Temperature Range (unless otherwise noted) (see section 3.1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MAX}	Maximum input clock frequency		340	-	MHz
t_{PDM}	Propagation delay	Clock to output (see NOTE 1)	1.41	2.15	ns
t_{PDMSS}	Propagation delay, simultaneous switching	Clock to output (see NOTES 1 and 2)	-	2.25	ns
t_{PD}	Propagation delay	CK and $\overline{\text{CK}}$ to PPO	.5	1.8	ns
t_{LH}	Low-to-High Delay	CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$	1.2	3	ns
t_{HL}	High-to-Low Delay	CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$	1	3	ns
t_{PLH}	Low-to-High propagation delay	$\overline{\text{RESET}}$ to $\overline{\text{PTYERR}}$	-	3	ns
t_{PHL}	Propagation delay	Reset to output	-	3	ns

NOTE 1 Includes 350 ps of test-load transmission line delay.

NOTE 2 This parameter is not necessarily production tested.

2.13 Output Buffer Characteristics

Table 12 — Output Edge Rates over Recommended Operating Free-air Temperature Range (see section 3.2)

Symbol	Parameter	Conditions	Min	Max	Unit
dV/dt_r	rising edge slew rate		1	4	V/ns
dV/dt_f	falling edge slew rate		1	4	V/ns
dV/dt_Δ [1]	absolute difference between dV/dt_r and dV/dt_f		-	1	V/ns

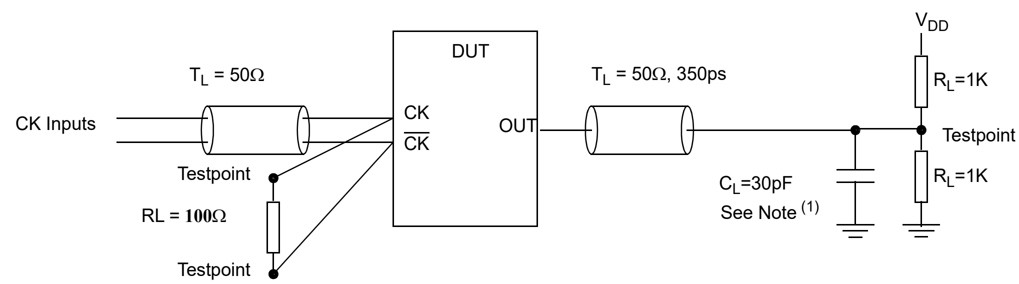
NOTE 1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

3 Test Circuits and Switching Waveforms

3.1 Parameter Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

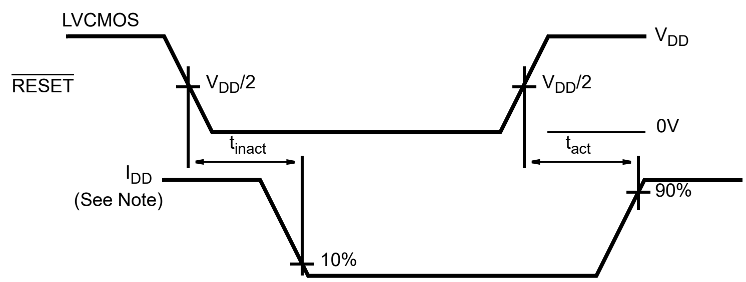
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



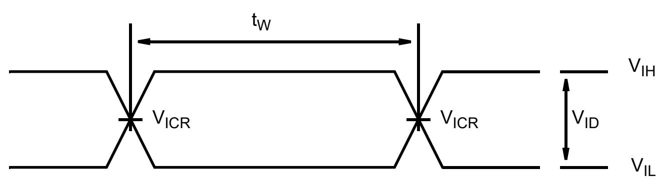
(1) C_L includes probe and jig capacitance.

Figure 9 — Load Circuit



I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Figure 10 — Voltage and Current Waveforms; Inputs Active and Inactive Times

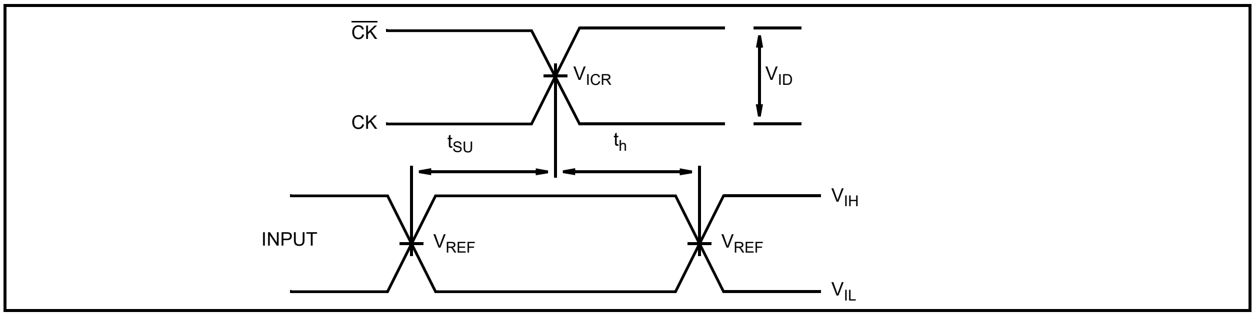


V_{ID} = 600 mV
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 11 — Voltage Waveforms; Pulse Duration

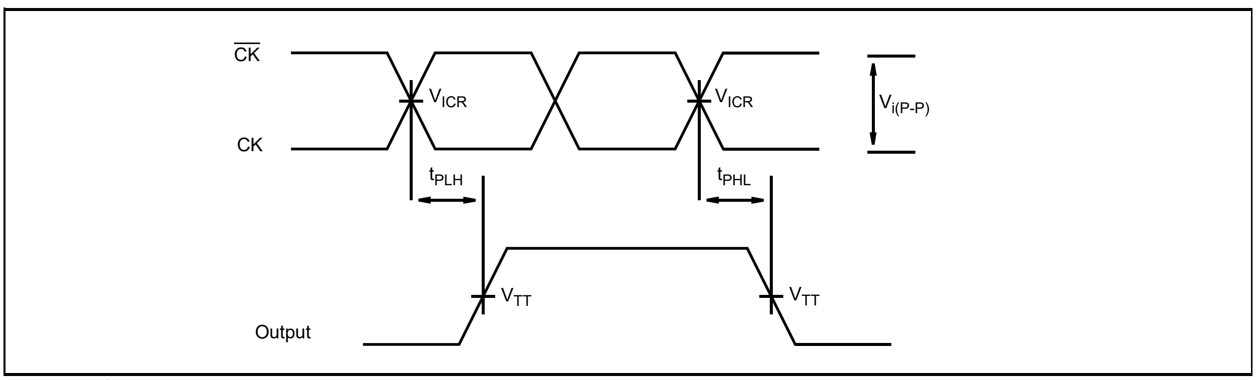
3 Test Circuits and Switching Waveforms (cont'd)

3.1 Parameter Measurement Information (cont'd)



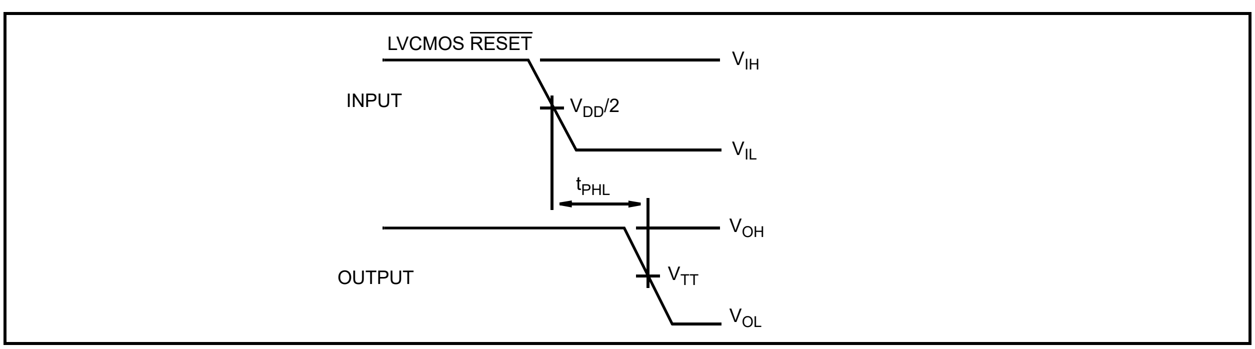
V_{ID} = 600 mV
$V_{REF} = V_{DD}/2$
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ − 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 12 — Voltage Waveforms; Set-up and Hold Times



$V_{TT} = V_{DD}/2$
V_{ICR} Cross Point Voltage
$V_{i(P-P)}$ = 600mV
t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 13 — Voltage Waveforms; Propagation Delay Times



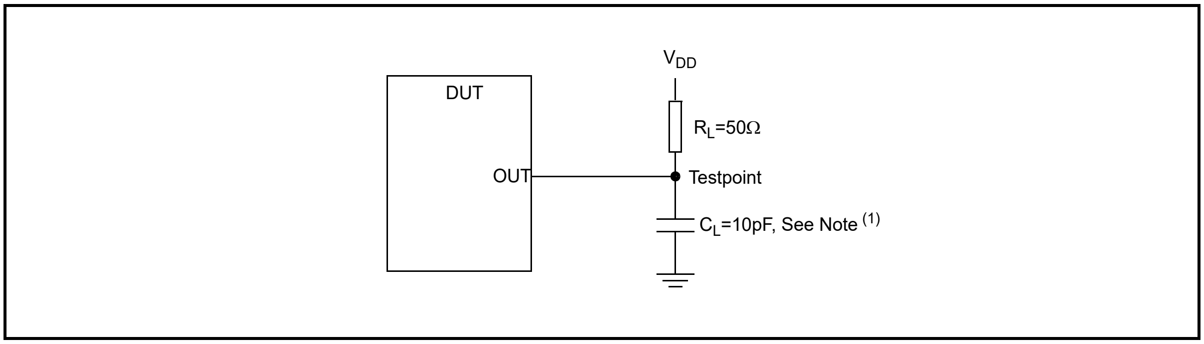
$V_{TT}=V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}.
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ − 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 14 — Voltage Waveforms; Propagation Delay Times

3 Test Circuits and Switching Waveforms (cont'd)

3.2 Output Slew Rate Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 15 — Load Circuit, HIGH-to-LOW Slew Measurement

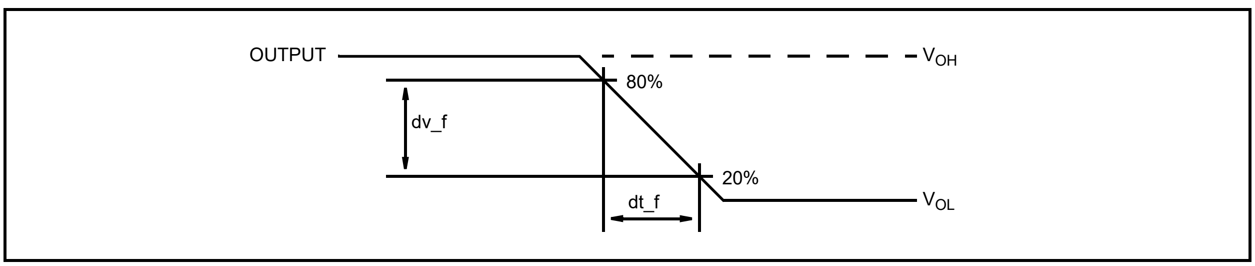
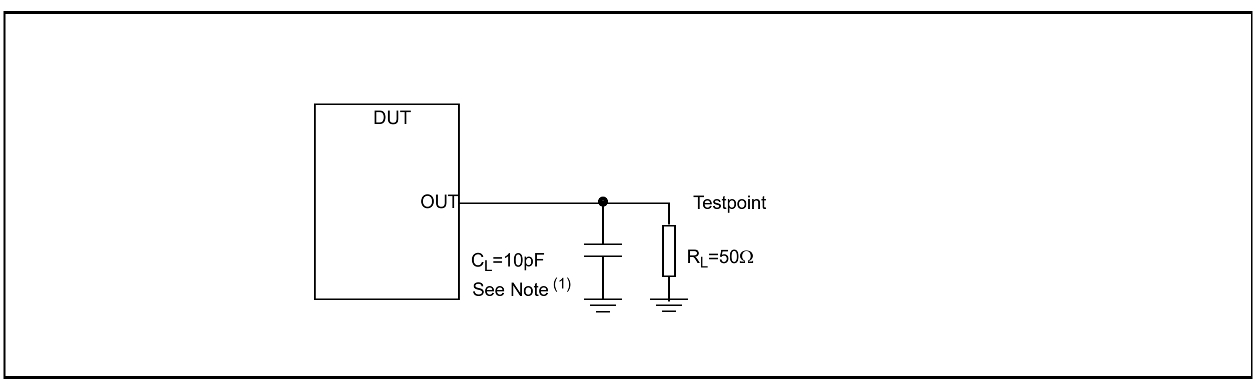


Figure 16 — Voltage Waveforms, HIGH-to-LOW Slew Rate Measurement



(1) C_L includes probe and jig capacitance.

Figure 17 — Load Circuit, LOW-to-HIGH Slew Measurement

3 Test Circuits and Switching Waveforms (cont'd)

3.2 Output Slew Rate Measurement Information (cont'd)

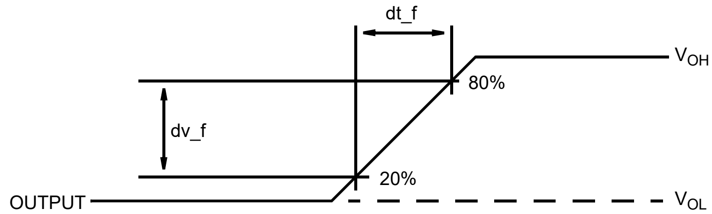
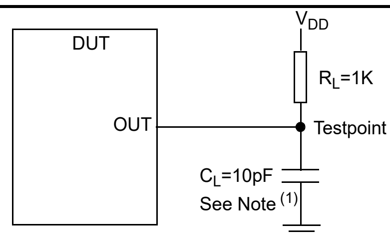


Figure 18 — Voltage Waveforms, LOW-to-HIGH Slew Rate Measurement

3.3 Error Output Load Circuit and Voltage Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 19 — Load Circuit, $\overline{\text{PTYERR}}$ Outputs

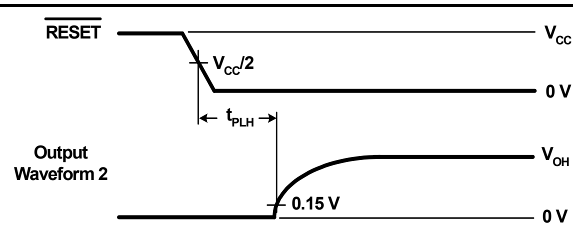
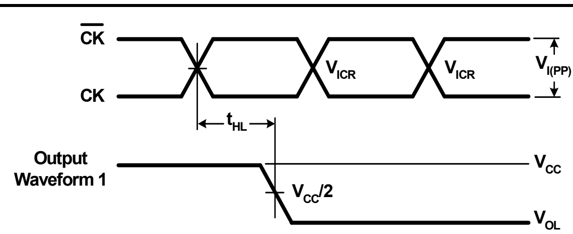


Figure 20 — Voltage Waveforms, Reset to $\overline{\text{PTYERR}}$ t_{PLH} Measurement



(1) C_L includes probe and jig capacitance.

Figure 21 — Load Circuit, CLK to $\overline{\text{PTYERR}}$ t_{PHL} Measurement

3 Test Circuits and Switching Waveforms (cont'd)

3.3 Error Output Load Circuit and Voltage Measurement Information (V_{DD} = 1.8 V±0.1 V) (cont'd)

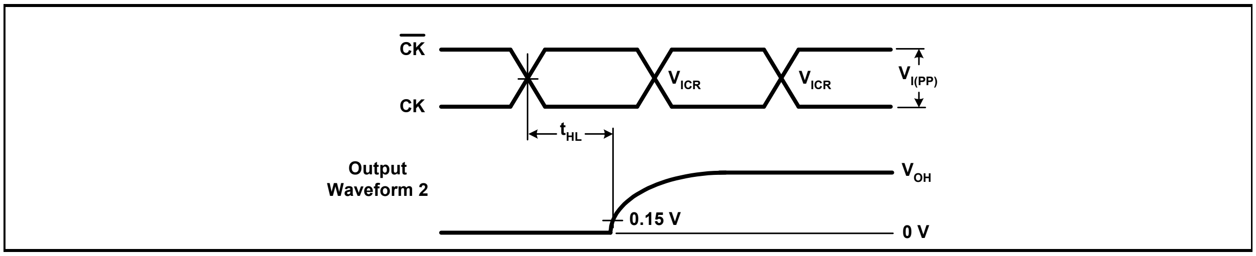
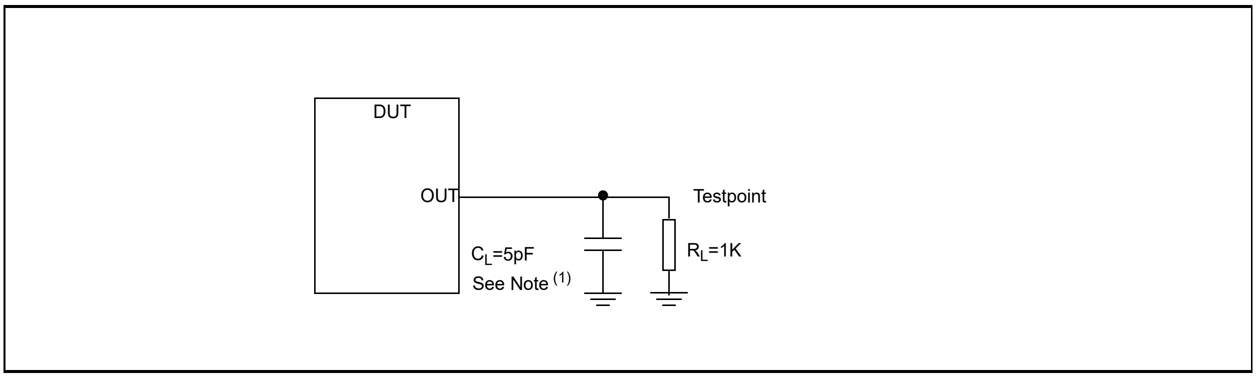


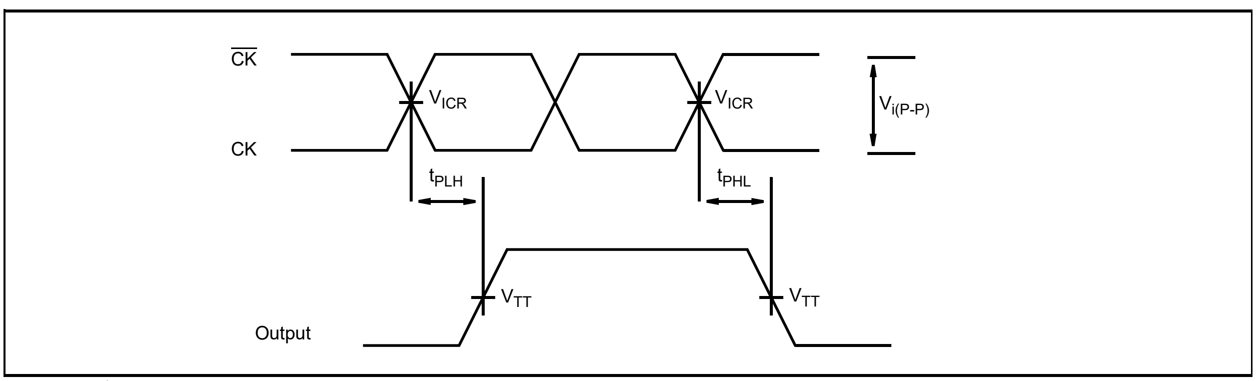
Figure 22 — Voltage Waveforms, CLK to $\overline{\text{PTYERR}}$ t_{PLH} Measurement

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 23 — Partial Parity Out Load Circuit

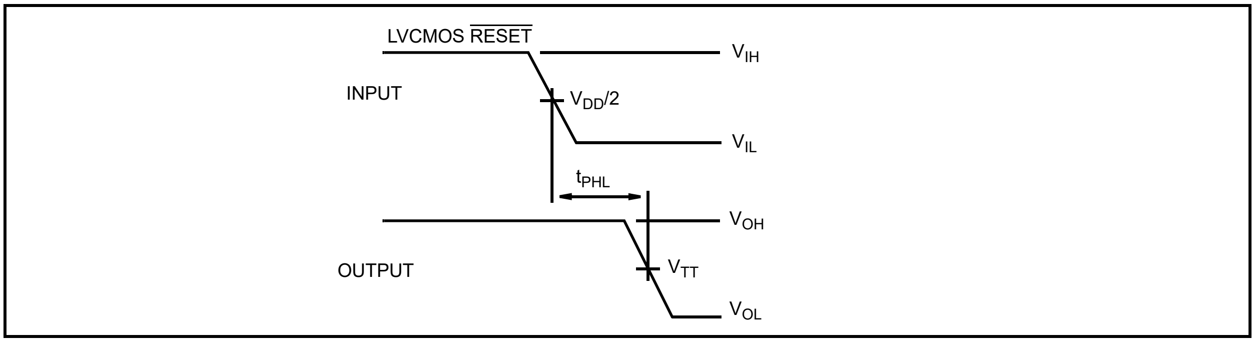


$V_{TT} = V_{DD}/2$
V_{ICR} Cross Point Voltage
$V_{i(P-P)}$ = 600mV
t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 24 — Partial Parity Out Voltage Waveform, Propagation Delay Time with Respect To CLK Input

3 Test Circuits and Switching Waveforms (cont'd)

3.3 Error Output Load Circuit and Voltage Measurement Information (V_{DD} = 1.8 V±0.1 V) (cont'd)



$V_{TT}=V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}.
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ − 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 25 — Voltage Waveforms; Propagation Delay Times

4 Reference to Other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*
- JESD8-7, *1.8V +/- 0.15V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Non terminated Digital Integrated Circuits.*
- JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18).*
- JESD21-C, *Configuration for Solid State Memories.*
- JESD82-7, *Definition of the SSTU32864 1.8 V Configurable Registered Buffer for DDR-II RDIMM Applications*

Annex A — (Informative) Differences between JESD82-12A and JESD82-12

This table briefly describes most of the changes made to entries that appear in this standard, JESD82-12A, compared to its predecessor, JESD82-12 (November 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page **Description of change**

This information was not provided by the sponsor at time of publication.

Annex B — (Informative) Differences between JESD82-12A.01 and JESD82-12A

Editorial changes as follows:

1. Terminology update: Changed “master” to “main” in Table 1 definition of CK and $\overline{CK}$ Clock Inputs
2. Updated JEDEC logos and Standard Improvement Form
3. All section headings, table titles, and figure titles changed to Initial Caps

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Standard Improvement Form **JEDEC Standard JESD82-12A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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